Amendments to the Claims:

This listing of claims replaces all prior versions, and listings, of claims in the application.

Listing of claims:

1. (Currently Amended) A main word line driver circuit of a semiconductor memory device, the circuit generating main word line signals enabling a plurality of main word lines, respectively, comprising:

a voltage supply unit which supplies a first voltage to a first node during a first time interval and then supplies a second voltage higher than the first voltage to the first node for a second time interval later than the first time interval; and

a plurality of output units connected to the first node which receive the first voltage and the second voltage supplied to the first node, each of the output units receiving a precharge signal and a respective decoded row address signal and comprising a second node inverted by an inverter to generate a respective main word line signal output by the output unit, the second node being connected to the first node through a transistor in response to the respective decoded row address signal such that the second node receives through the transistor the first and second voltages generated by the voltage supply unit in response to the respective decoded row address signal, each output unit, in response to the precharge signal and the respective decoded row address signal and the first and second voltages, generating ~~and generate~~ the respective main word line signal[[s]].

2. (Currently Amended) The circuit of claim 1, wherein the first voltage is a negative voltage and the second voltage is [[the]] ground voltage.

3. (Currently Amended) The circuit of claim 2, wherein the voltage supply unit comprises:

a negative voltage supply unit which supplies the negative voltage to the first node; and

a ground voltage supply unit which supplies the ground voltage to the first node.

4. (Currently Amended) The circuit of claim 3, wherein the negative voltage supply unit supplies the negative voltage to the first node in response to activation of decoded row address signals.

5. (Currently Amended) The circuit of claim 4, wherein one of the decoded row address signals is activated as the supply voltage for ~~a predetermined~~ the first time interval.

6. (Original) The circuit of claim 5, wherein the negative voltage supply unit comprises three NMOS transistors which are serially connected and turned on/off in response to the decoded row address signals, and the negative voltage is connected to an end of the NMOS transistors.